

# COPY

RESPONSE UNDER 37 C.F.R. § 1.111  
Serial Number: 09/896,523  
Filing Date: April 29, 2001  
Title: VOLTAGE-LEVEL CONVERTER  
Assignee: Intel Corporation

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## IN THE CLAIMS

No claims are currently amended.

1. - 28. (Canceled)

29. (Previously Presented) A voltage-level converter comprising:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, wherein the static voltage-level converter includes two down-sized transistors.

30. (Previously Presented) The voltage-level converter of claim 29, wherein the two down-sized transistors are insulated gate field-effect transistors.

31. (Previously Presented) A voltage-level converter comprising:

a static voltage-level converter including at most four transistors and an inverter coupled to no more than two transistors in the static voltage-level converter each of the no more than two transistors directly coupled to a voltage level; and

a split-level output circuit coupled to the static voltage-level converter, wherein the static voltage-level converter comprises:

an input node, a first output node, and a second output node;

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node; and

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node, wherein the inverter is

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coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node, wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are down-sized.

32. (Previously Presented) The voltage level converter of claim 31, wherein the second transistor of the first pair of transistors and the second transistor of the second pair of transistors are insulated gate field-effect transistors.